Line Loop Back for Very High Speed Application

ABSTRACT OF THE DISCLOSURE

Method and circuitry for performing a line loop back test includes a receiver, a deserializer, and a low speed parallel loop back data multiplexer selects either the low speed parallel data from the deserializer when in loop back mode or low speed parallel input data when in normal mode. The deserializer produces a low speed clock output signal that is fed to a low speed loop back reference clock multiplexer and also to a low speed loop back clock multiplexer. Both the loop back reference clock multiplexer and the loop back clock multiplexer select the low speed clock output signal from the deserializer when in line loop back mode. A clock multiplying unit converts the output of the low speed loop back reference clock multiplexer into a high speed clock signal. The serializer generates the high speed serial transmitter data in synchronization with the high speed clock signal received from a clock multiplying unit. A clock divider circuit converts the high speed clock signal from the clock multiplying unit into a low speed FIFO output clock. A first-in-first-out buffer receives the low speed parallel output data in synchronization with a clock multiplexer output, and transmits low speed parallel FIFO data to the serializer in synchronization with the low speed FIFO output clock. A low speed parallel loop back data buffer provides coupling between the deserializer and the low speed parallel loop back data multiplexer, and a low speed loop back clock buffer provides coupling between the deserializer and the loop back reference clock multiplexer and the loop back clock multiplexer.